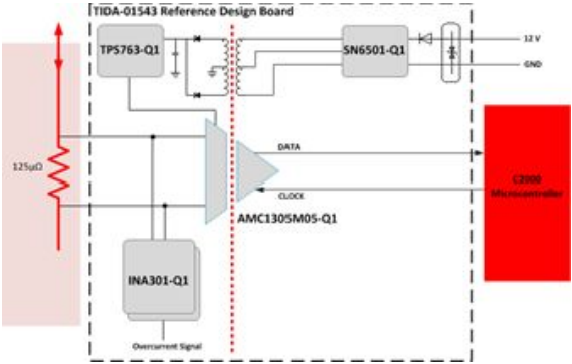
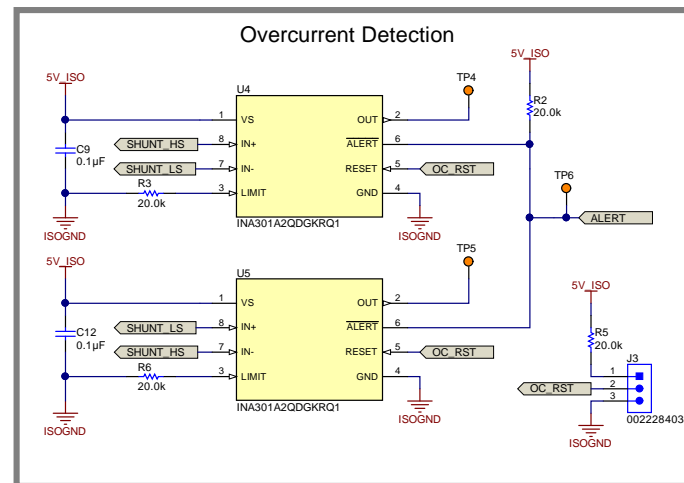
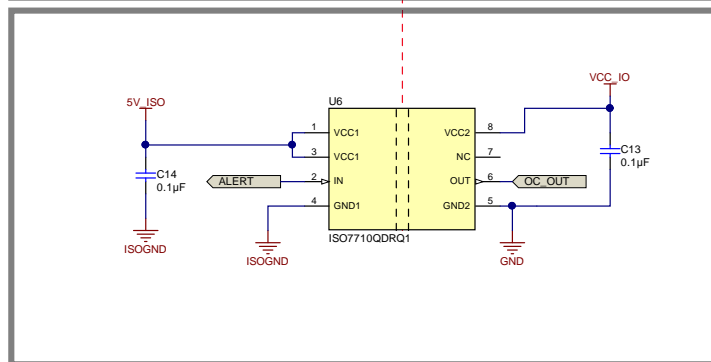
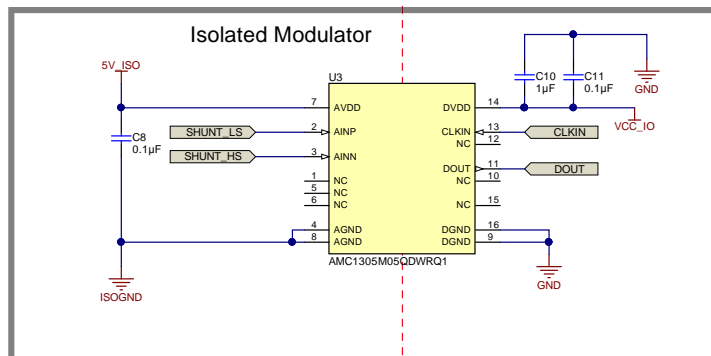
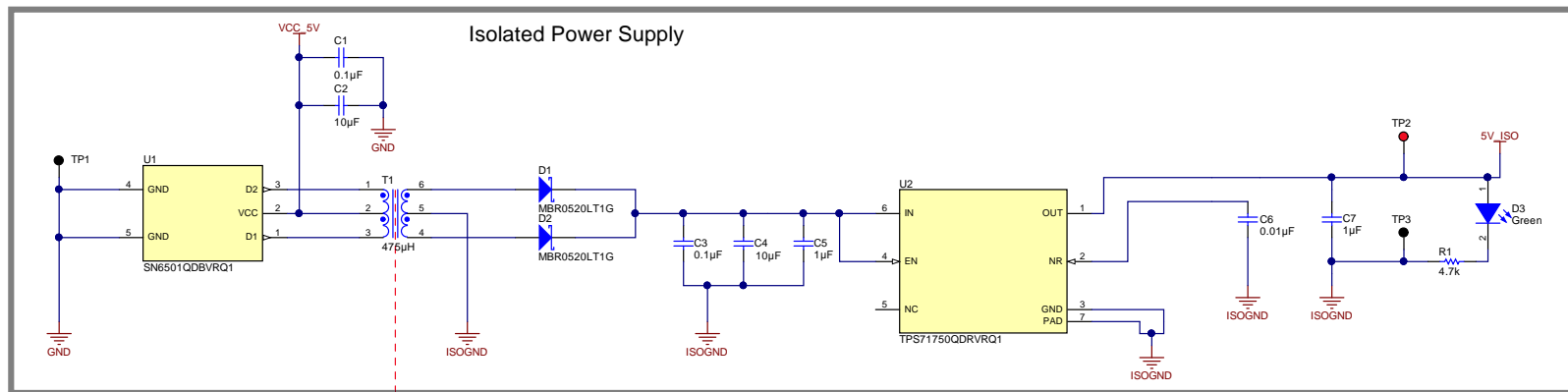


Revision History				
Rev	ECN #	Approved Date	Approved by	Notes
N/A	N/A	N/A	N/A	N/A





Note: R3 and R6 set the current at which the ALERT output is activated.
See the INA301 Datasheet for more Information.

80 uA current source in the INA, with R_Limit=20k
INA Threshold: 1.6V at Output
 $1.6V/50 = 32mV$ at INA input
Overcurrent detection triggers at +256A with 125 uOhm shunt

H1 1
NY PMS 440 0025 PH

H2 1
NY PMS 440 0025 PH

H3 1
NY PMS 440 0025 PH

H4 1
NY PMS 440 0025 PH

H5
1902C

H6
1902C

H7
1902C

H8
1902C

FID1

FID2

FID3

PCB Number: TIDA-01543
PCB Rev: A1

PCB
LOGO

PCB
LOGO

You should delete the nylon screws/standoffs and/or the bumpers as needed for your design (or substitute other parts from Hardware.IntLib). Bumpers are cheaper, but provide less clearance.

Deleting anything else from this page may result in your EVM submission being rejected (until you add them back).

Update the Label Text in the Label Table as needed for each Assembly Variant.

You should delete this note too.

Variant/Label Table

Variant	Label Text
001	ChangeMe!
002	ChangeMe!

LBL1

PCB Label

Size: 0.65" x 0.20"

ZZ1

Label Assembly Note

This Assembly Note is for PCB labels only

ZZ2

Assembly Note

This Assembly Note will show in the PcbDoc and associated outputs

ZZ3

Assembly Note

This Assembly Note will show in the PcbDoc and associated outputs

ZZ4

Assembly Note

This Assembly Note will show in the PcbDoc and associated outputs

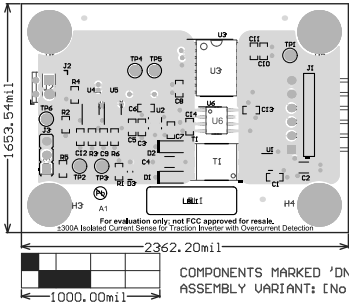
A

B

C

D

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
Z22 ■ This Assembly Note will show in the PcbDoc and associated outputs
Z23 ■ This Assembly Note will show in the PcbDoc and associated outputs
Z24 ■ This Assembly Note will show in the PcbDoc and associated outputs



Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric1	FR-4 High Tg	18.00mil	4.2	
5	GND	Copper	1.42mil		
6	Dielectric 2	FR-4 High Tg	20.00mil	4.2	
7	PWR	Copper	1.42mil		
8	Dielectric 3	FR-4 High Tg	18.00mil	4.2	
9	Bottom Layer	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 10 MIL
MIN. CLEARANCE: 2.874 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
☐ FR-408 ☒ FR-4 High Tg ☐ OTHER
THICKNESS: ☒ 62 MIL (1.6mm) +/-10% ☐ OTHER
TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/-
BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/-

DRILLING:
REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES
PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER

BOARD FINISH:
SILKSCREEN: ☒ TOP ☐ BOTTOM
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER
SOLDER RESIST COLOR: ☒ GREEN ☐ OTHER
☒ MATTIE ☐ SEMI-GLOSS
SURFACE FINISH: ☒ IMMERSION GOLD (ENG) ☐ ENERP
☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER
ARRAY/PANEL: ☐ CUT AND TRM PER M1 BOARD OUTLINE
☐ N.C. ROUTE ☒ V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs
TO MEET OR EXCEED THE REQUIREMENTS OF:
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3
☒ RoHS ☐ OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: ☐ YES
BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER
☐ XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
☐ XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
☐ OUTER XX MIL VIAS REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
☐ LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE
TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PROJECT TITLE:
s300A Isolated Current Sense for Traction Inverter with Overcurrent Detection

DESIGNED FOR:
Public Release

FILE NAME:
PCB_PcbDoc

ENGINEER:
S. M.

LAYOUT BY:
S. M.

SCALE: 1.00

ALTUM DESIGNER VERSION:
17.1.5.472

ADDITIONAL COMMENTS	IA	BOARD #	DATE	AI	SUN	DATE	DATE
LAYER NAME = Top Overlay		TID #:	N/A	AI	#	QIT	DATE
PLT/INSTRUMENTS		GENERATED	7/2/2019	2:46:16 PM			

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1

2

3

4

5

6